Abstracts

Reference Plane Parasitics Modeling and Their Contribution to the Power and Ground Path "Effective" Inductance as Seen by the Output Drivers

R. Senthinathan, A.C. Cangellaris and J.L. Prince. "Reference Plane Parasitics Modeling and Their Contribution to the Power and Ground Path "Effective" Inductance as Seen by the Output Drivers." 1994 Transactions on Microwave Theory and Techniques 42.9 (Sep. 1994, Part II [T-MTT]): 1765-1773.

Modeling of the current distribution in package reference (power and ground) planes and the extraction of the associated parasitic are presented. Electrical network and equivalent circuit are developed to model the chip-package interface including the effects of V/sub DD//V/sub SS/ planes. For single- and multichip packages, methods of calculating the "effective" inductance (L/sub eff/) as seen by the output drivers from their on-chip V/sub DD/ and V/sub SS/ buses to the tip of the package pin are explained. Variations from the conventional method (where all connections are assumed identical) of calculating L/sub eff/ are analyzed. Closed-form equations are given to estimate the simultaneous switching noise (SSN) on the on-chip V/sub DD//V/sub SS/ buses for packaged CMOS circuits. The contribution of reference plane (with and without perforation) parasitic on the SSN are investigated. Optimal package pin placement to minimize the plane inductance is discussed.

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